REMARKS

Applicant has considered the Non-Final Office Action dated July 8, 2009 and the references cited therein. Claims 1, 3-8 and 16-19 were previously pending. No claims have been allowed. Applicant has amended claims 1 and 8 to address the prior art-based grounds for rejection set forth in the Office Action. Applicant has amended Claims 3-7 to address the Claim objection presented in sections 6-7 of the Office Action. New Claim 20 corresponds to previously canceled claim 2 (when claim 2 was incorporated into claim 1 in the RCE amendment).

Applicant has amended the previously rejected independent claims 1 and 8 by incorporating claim 4 (in corrected form to address the claim objection) into claim 1 and a (narrower) version of claim 9 into claim 8.

For the reasons set forth herein below, Miller neither discloses nor suggests each of the recited elements of independent claims 1 or claim 8 and, by definition, all the elements of dependent claims 2-3, 5-8 and 16-19. Applicant provides particular reasons for traversing the prior art-based claim rejections herein below.

Applicant requests favorable reconsideration of the Office Action's ground for rejecting the previously pending claims in view of Applicant's remarks provided herein below. Please charge any fee deficiencies to Deposit Account No. 12-1216.

Summary of the Claim Rejections

1. Claims 1, 3-8 and 16-19 are rejected under 35 U.S.C. § 112 second paragraph as being indefinite for failing to particularly point out and distinctly claim the subject-matter which regards as the invention.

2. Claims 1, 3-4, 6-8 and 16-19 are rejected under 35 U.S.C. § 103(a) as being obvious over Miller et al. U.S. Pat. No. 5,819,058 (Miller).

3. Claim 5 is rejected under 35 U.S.C. § 103(a) as being obvious over Miller in view of Keller et al. U.S. Pat. No. 6,546,478 (Keller).

Applicant traverses the grounds for each and every rejection of the previously pending claims in view of the current amendments and for at least the reasons set forth herein below. Applicant addresses the specific rejections in the order they arise in the Office Action.

Applicant's Detailed Remarks Addressing the Claim Rejections

1. Rejection of claims 1, 3-8 and 16-19 under Section 112, paragraph 2

The Office Action, at section 12, objects to the use of "prefetching" in claims 1, 3, 17 and 19. The Office Action asserts that what is claimed isn't prefetching as understood to one of ordinary skill in the art. Instead, the Office Action states that the described act is simply "fetching" data when the data is needed. Applicant has now replaced the term "prefetch" with "fetch" in each of the rejected claims 1, 3, 17 and 19 (and new claim 20 which corresponds to previously canceled claim 2).

The Office Action, at section 13, rejects claim 6 for reciting a claim element having no antecedent basis (for "the functional units" in line 3). As a correction Applicants replaced "the functional units" by "different functional units," which is the wording used in paragraph 19 of the Application specification as filed.

2. Rejection of Claims 1, 3-4, 6-8 and 16-19 as being unpatentable over Miller (and claim 5 being obvious over Miller in view of Keller)

Applicant specifically traverses the rejection of presently pending independent **claims 1 and 8** (corresponding to previously pending **claims 4 and 9**) as being unpatentable over Miller. Claim 1 has been amended to, among other things, incorporate elements of previously pending claim 4 (now canceled). Claim 8 is amended to incorporate part of the recited claim elements (joined by an "or" connector) in previously canceled claim 9 (which was previously incorporated into claim 8) thereby narrowing claim 8.

Applicant's Claimed Invention

Applicant's amended independent computer **system claim 1** includes a processing unit and a memory (*see*, FIG. 3). The processing unit is arranged to fetch memory lines from the memory and execute instructions from the memory lines (*see*, FIG. 2, page 9, lines 29-31). Each memory line is fetched as a whole and is capable of holding more than one instruction.

Moreover, at least one instruction from the memory line comprises information, inserted at compile time, that signals explicitly how the processing unit, when processing the instruction from a current memory line, should control how a part of processing is affected by crossing of a boundary to a subsequent memory line (*see,* FIG. 2). Examples include stall, realign and prefetch bits (*see*, page 11, lines 25-33). The processing unit responds to the aforementioned information by controlling the part of processing (as signaled by the information)

With regard to the (amended) portion of claim 1 incorporated from (now-canceled) claim 4, the information inserted at compile time explicitly signals whether to update an instruction pointer from a position behind the instruction in the current memory line to a start of the subsequent memory line, so that information following the instruction on the current memory line *is skipped over*. The processing unit is arranged to update the instruction pointer to the start of the subsequent memory line in response to the information (*see, e.g.,* Applicant's published application at paragraphs 73 and 84).

Amended independent **method claim 8**, including similar recited elements, is supported by substantially the same portions of the disclosure recited above with regard to amended computer system claim 1.

The Cited Miller Patent

Miller discloses a system and method for compressing and decompressing variable length instructions contained in variable length instruction packets executed by a processor having a plurality of processing units.

Regarding compression, Miller discloses a compression system including:

- a component for generating an instruction packet containing a plurality of instructions, and
- a component for assigning a compressed instruction having a predetermined length to an instruction within the instruction packet.

Miller discloses a shorter compressed instruction corresponding to a more frequently used instruction. Miller also discloses a component for generating an instruction packet containing compressed instructions for corresponding ones of the plurality of processing units.

Regarding decompression, Miller discloses a decompression system including a component for storing a plurality of the instruction packets in a plurality of storage locations. A further component in Miller's system generates an address pointing to a selected variable length instruction packet in the storage system, and a decompression component for decompressing the compressed instructions in the selected instruction packet to generate a variable length instruction for each of the processing units.

Miller's disclosed system potentially includes a component for routing the variable length instructions from the decompression system to each of processing units. *See,* Miller, Abstract.

Miller's execution control unit (ECU) 26 controls retrieval and execution of instructions within the VLIW processor. *See*, Miller, col. 4, lines 1-2 and column 8, lines 22-24. The compressed instructions comprise a stop bit (or an end of packet EP/NEP bit) that indicates to the ECU 26 and processor where one compressed instruction packet ends and a next compressed instruction packet begins. *See,* Miller, column 5, lines 34-38. Accordingly the ECU 26 calculates a length of a present instruction from an end of packet indicator. The ECU 26 also calculates the start address of the next instruction.

Miller uses a dual memory and a particular alignment so that a following instruction can be fetched in a single cycle. *See,* Miller, column 10, line 36 to column 11, line 2. Thus a complete instruction packet is always stored in a single address of the first memory and the second memory of the dual memory. Furthermore, the addresses for the memory banks are generated separately as Aleft and Aright, so that the addresses can be independently incremented. Miller states "However, in this system, the first and second memories are addressed in parallel to retrieve 128 bits so that instruction packets may cross the boundary between the memories." *See*, Miller, column 10, line 67 to column 11, line 2.

Importantly, Miller furthermore discloses a *pad instruction* to ensure that instruction packets larger than 80 bits are properly aligned within the instruction memory. The pad instruction 260 ensures that long instruction packets start at an appropriate boundary. The pad instruction is inserted into the instruction packet stream by the compression system and is then discarded by the decompression system. The pad instruction does not cause any operation to occur in the processing units. *See*, Miller, column 11, lines 35-43. Miller describes the effect of the pad instruction 260 as follows: "The addressing system then determines that the next instruction packet, IP4 is 128-bits long and also has a pad instruction in front of it. As the addressing system encounters the pad instruction, *it reads out the pad instruction* and discards it. Then, because the next instruction packet is 128-bits long, both the Aright and Aleft addresses are incremented so that the processor may access addresses 16, 17, 18, 19, 12, 13, 14, and 15." *See*, Miller, column 12, lines 10-14 (emphasis added).

Applicant's Specific Argument Traversing the Rejection of Amended Claim 1

Applicant traverses the rejection of currently amended **independent claim 1** (previously pending claim 4) since the disclosure of Miller would not have rendered the claimed invention obvious to one skilled in the art at the time of the invention. More particularly, Claim 1 recites:

> "at least one instruction from the memory lines comprising information, inserted at compile time, that signals explicitly how the processing unit, when processing the instruction from a current memory line, should control how a part of processing is affected by crossing of a boundary to a subsequent memory line, the processing unit being arranged to respond to the information by controlling said part of processing as signaled by the information"

Moreover Claim 1 also recites (from canceled claim 4):

> "wherein the information inserted at compile time signals explicitly whether or not an instruction pointer should be updated from a position behind the instruction in the current memory line to a start of the subsequent memory line, so that information following the instruction on the current memory line is skipped over, the processing unit being arranged to update the instruction pointer to the start of the subsequent memory line in response to the information."

The Office Action has not provided a *prima facie* case of obviousness with regard to previously pending claim 4 (whose recited elements now replace the elements of claim 2 that were previously incorporated into claim 1) since Miller fails to disclose at least one recited element of claim 1. In particular, Miller does not disclose "information inserted at compile time that signals explicitly whether or not an instruction pointer should be updated from a position behind the instruction in the current memory line to a start of the subsequent memory line, so that information following the instruction on the current memory line *is skipped over,* the processing unit being arranged to update the instruction pointer to the start of the subsequent memory line in response to the information." (emphasis added).

Moreover, not only does Miller lack at least the above recited element, Miller *teaches away from the missing recited element of claimed invention*, in that according to the teaching of Miller the "pad" instruction that is used to align the next instruction packet *is read out (i.e., considered and identified as a "pad" instruction), and then discarded. See*, Miller, column 12, lines 10-14. Skipping information involves completely disregarding it – i.e., not even reading it. If, as in Miller's system, a pad instruction is "read out" then "the information following the instruction" is not being "skipped over" (as recited in the presently pending claims) – rather, it is being read, identified, and processed as a "pad" instruction. **Applicant considers the above**

point regarding the difference between a "pad" instruction and Applicants' presently recited element of skipping to a subsequent memory line to be significant and request thoughtful consideration of this point of distinction.

Applicant submits that currently amended method **claim 8**, which incorporates the above-discussed "skip" functionality, is patentable over the prior art for at least the reasons stated herein above with regard to currently amended claim 1.

Moreover, Applicant traverses the rejection of each of the dependent claims (as either anticipated by Miller or obvious over the combined teachings of Miller and Keller) over the prior art for the reasons set forth for claims 1 and 8 from which each depends.

Conclusion

Applicant respectfully submits that the patent application is in condition for allowance. If, in the opinion of the Examiner, a telephone conference would expedite the prosecution of the subject application, the Examiner is invited to call the undersigned attorney.

Respectfully submitted,

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